FIG. 1

STRUCTURAL VIEW OF A WIRING DEVICE IN ONE EMBODIMENT

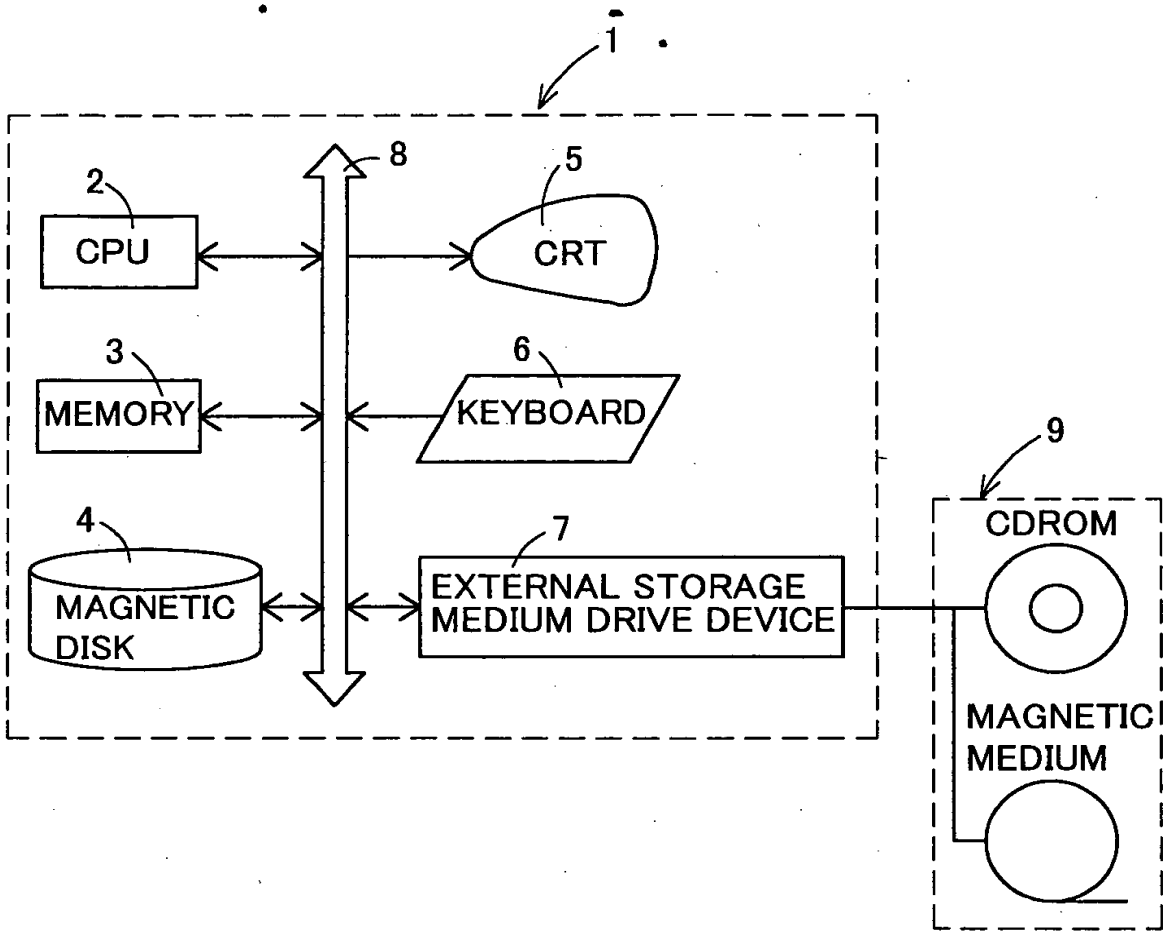


FIG. 2

PLAN VIEW SHOWING A CONNECTION BETWEEN METAL WIRING LAYERS IN THE EMBODIMENT

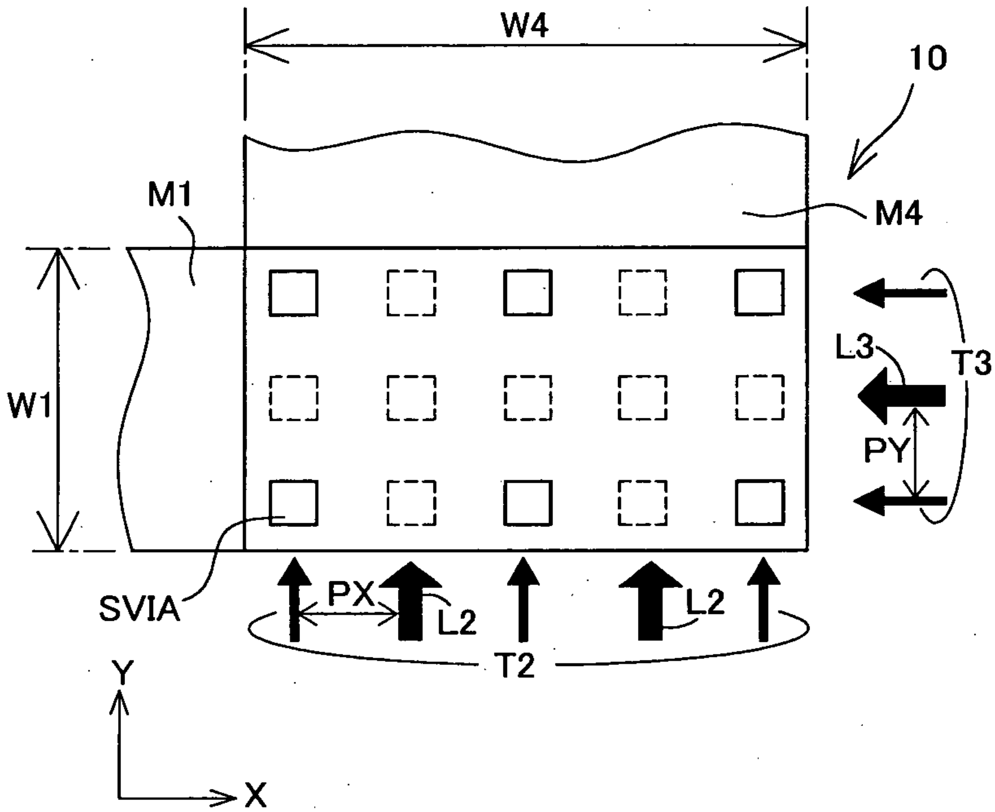
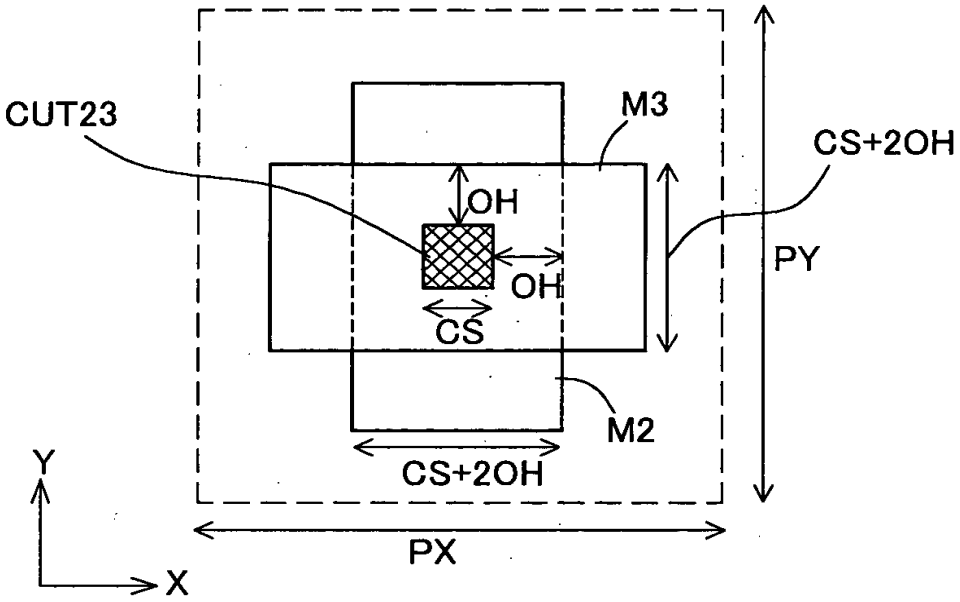


FIG. 3

PATTERN VIEW SHOWING AN INTERMEDIATE VIA IN A FIRST SPECIFIC EXAMPLE OF THE EMBODIMENT



(VIA23' = M2 + CUT23 + M3)

FIG. 4

PLAN VIEW SHOWING A CONNECTION BETWEEN METAL WIRING LAYERS IN THE FIRST SPECIFIC EXAMPLE OF THE EMBODIMENT

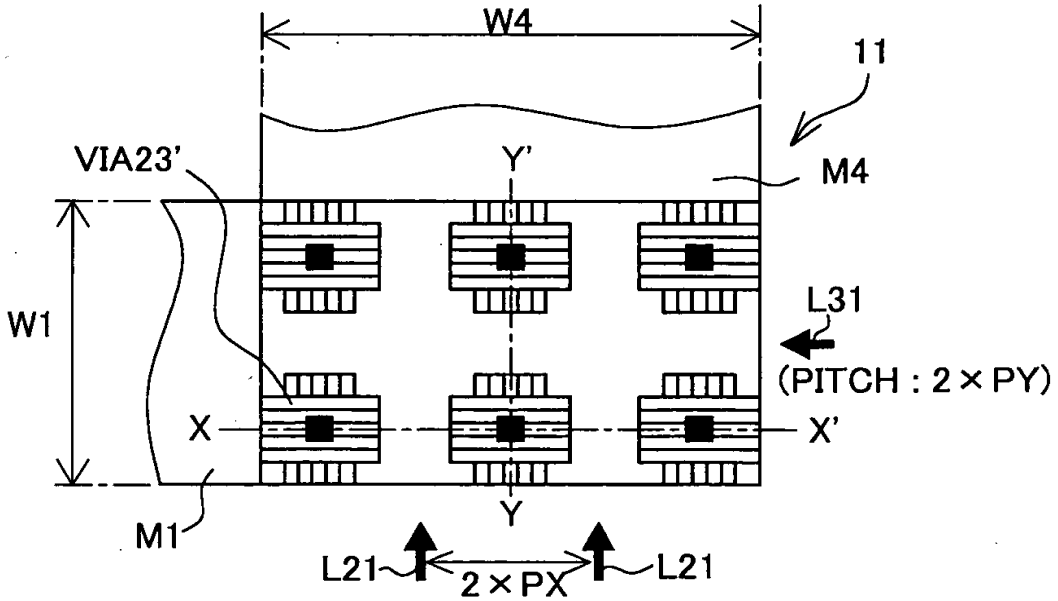
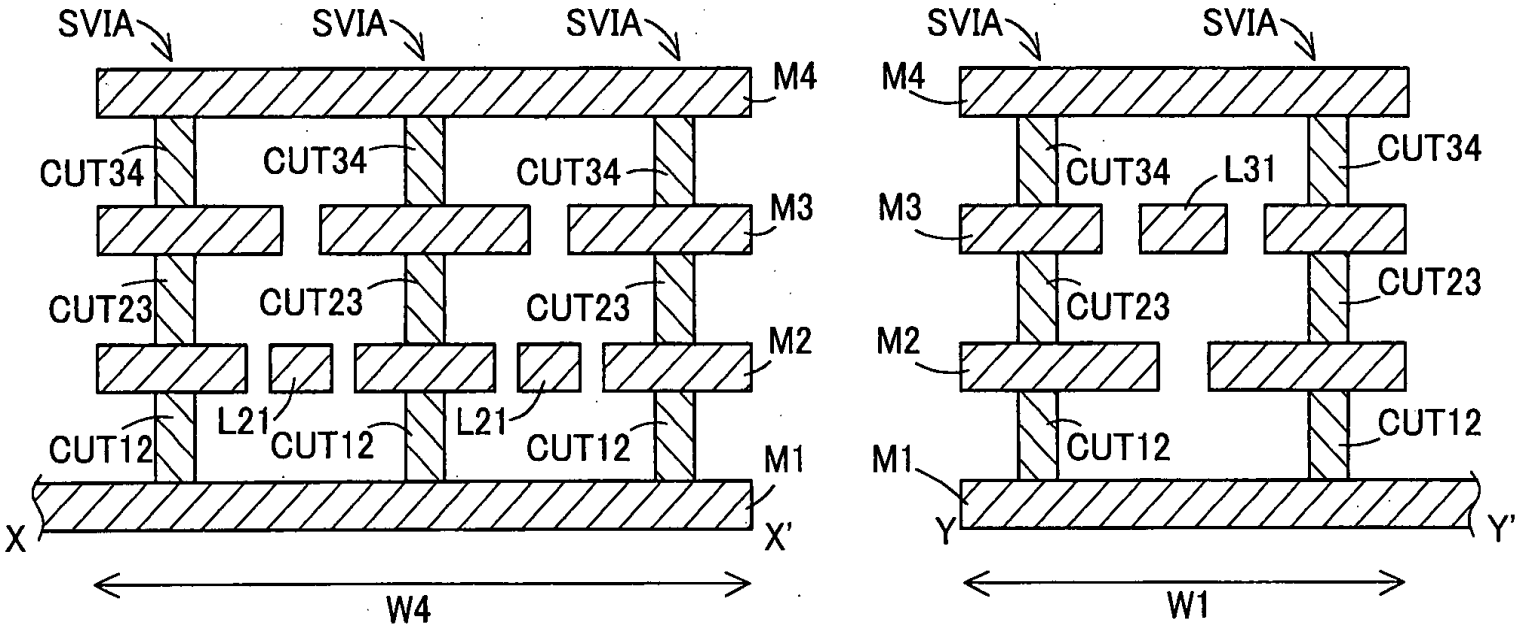


FIG. 5 CROSS-SECTIONAL VIEW SHOWING A CONNECTION BETWEEN METAL WIRING LAYERS IN THE FIRST SPECIFIC EXAMPLE OF THE EMBODIMENT



(A) X-X'CROSS SECTION

(B) Y-Y'CROSS SECTION

FIG. 6

PLAN VIEW SHOWING A CONNECTION BETWEEN METAL WIRING LAYERS IN A SECOND SPECIFIC EXAMPLE OF THE EMBODIMENT

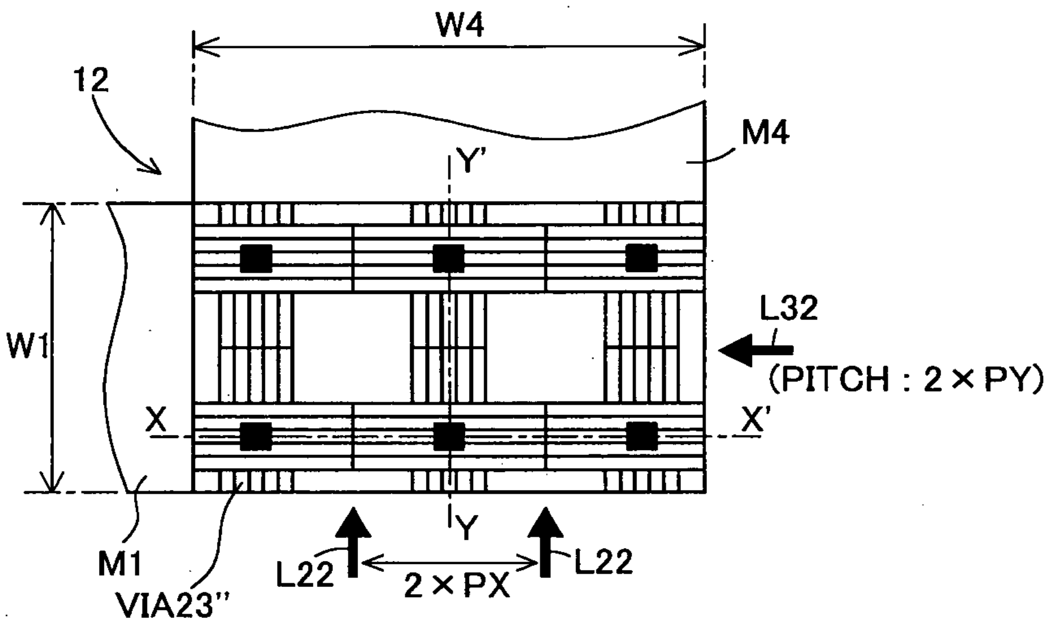
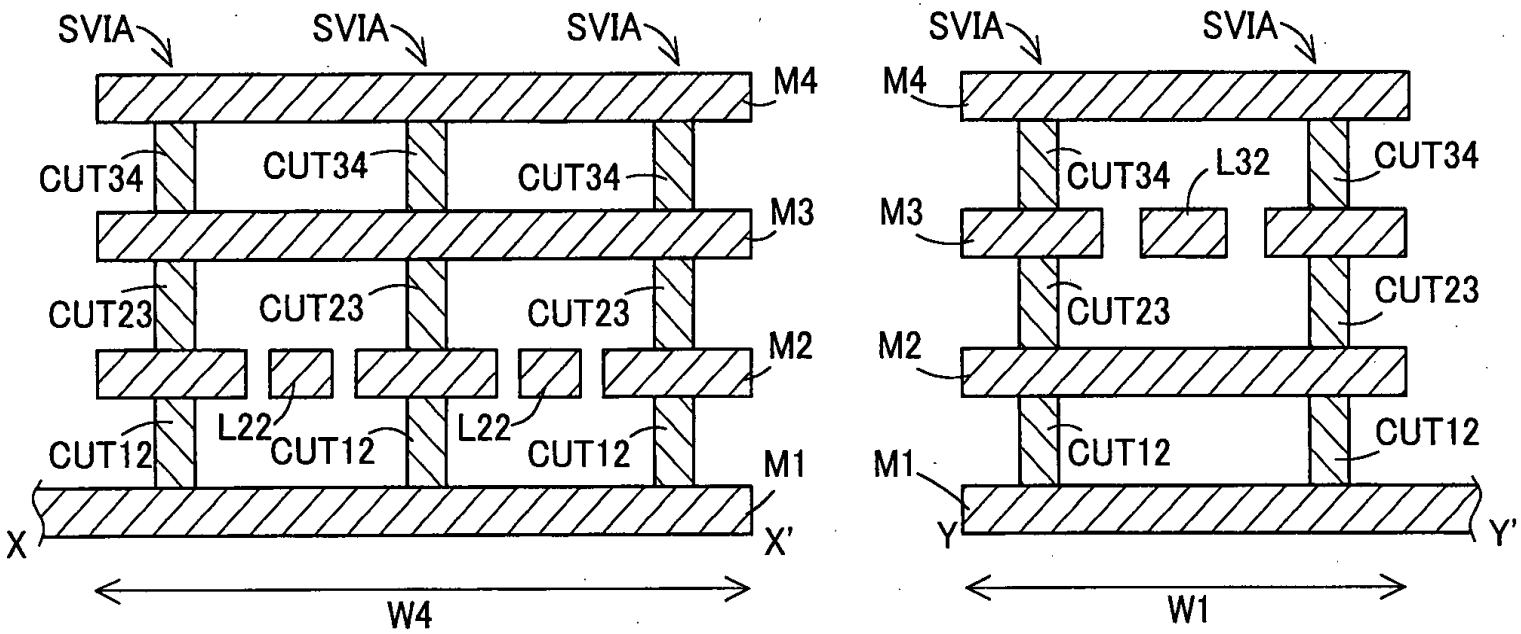


FIG. 7 CROSS-SECTIONAL VIEW SHOWING A CONNECTION BETWEEN METAL WIRING LAYERS IN THE SECOND SPECIFIC EXAMPLE OF THE EMBODIMENT



(A) X-X'CROSS SECTION

(B) Y-Y'CROSS SECTION

FIG. 8

FLOW CHART SHOWING A WIRING METHOD FOR AN INTERMEDIATE METAL LAYER PARTITIONING ROUTINE IN THE EMBODIMENT

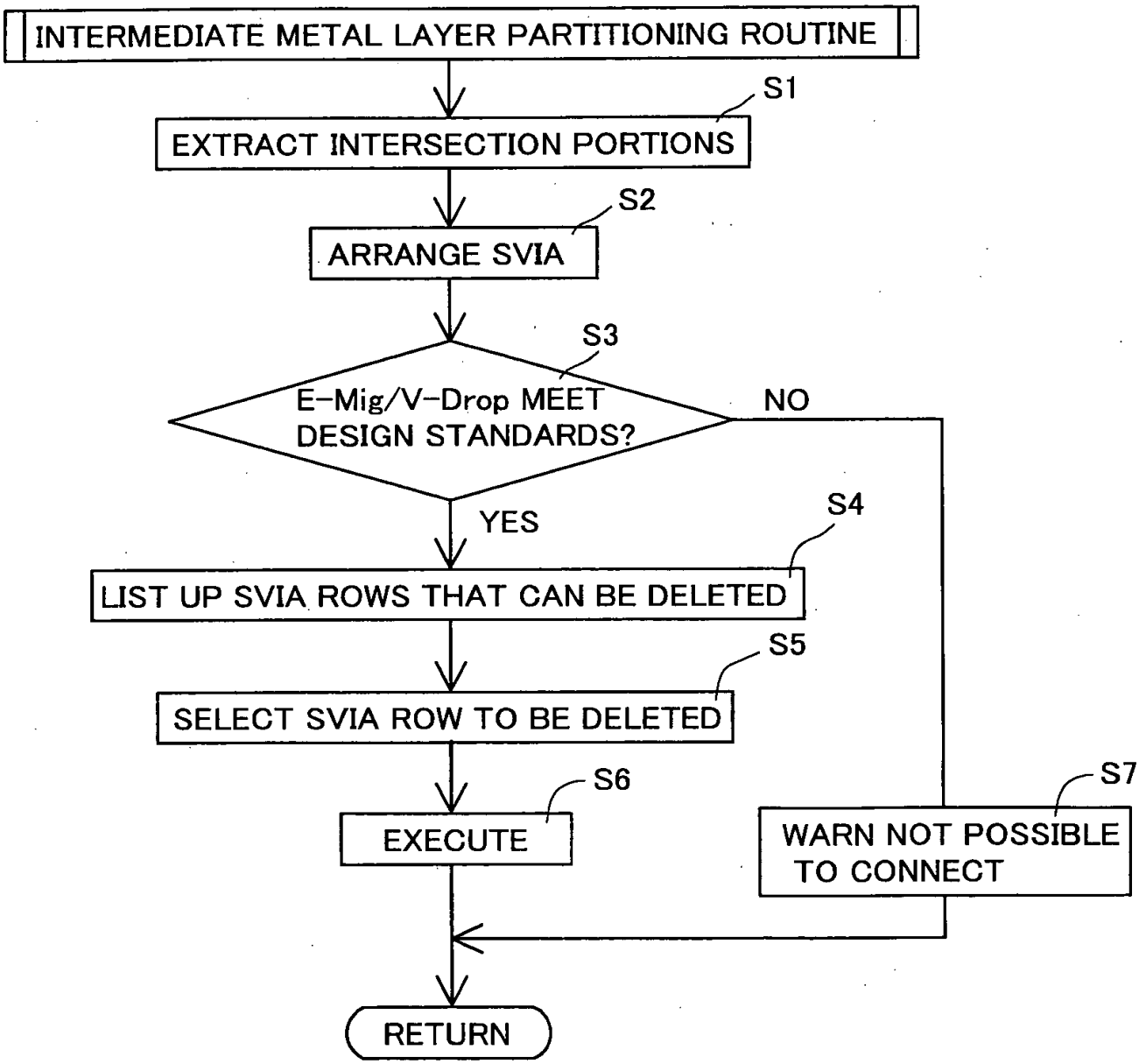


FIG. 9 CROSS-SECTIONAL VIEW OF A SEMICONDUCTOR DEVICE HAVING A MULTIPLE LAYER WIRING STRUCTURE

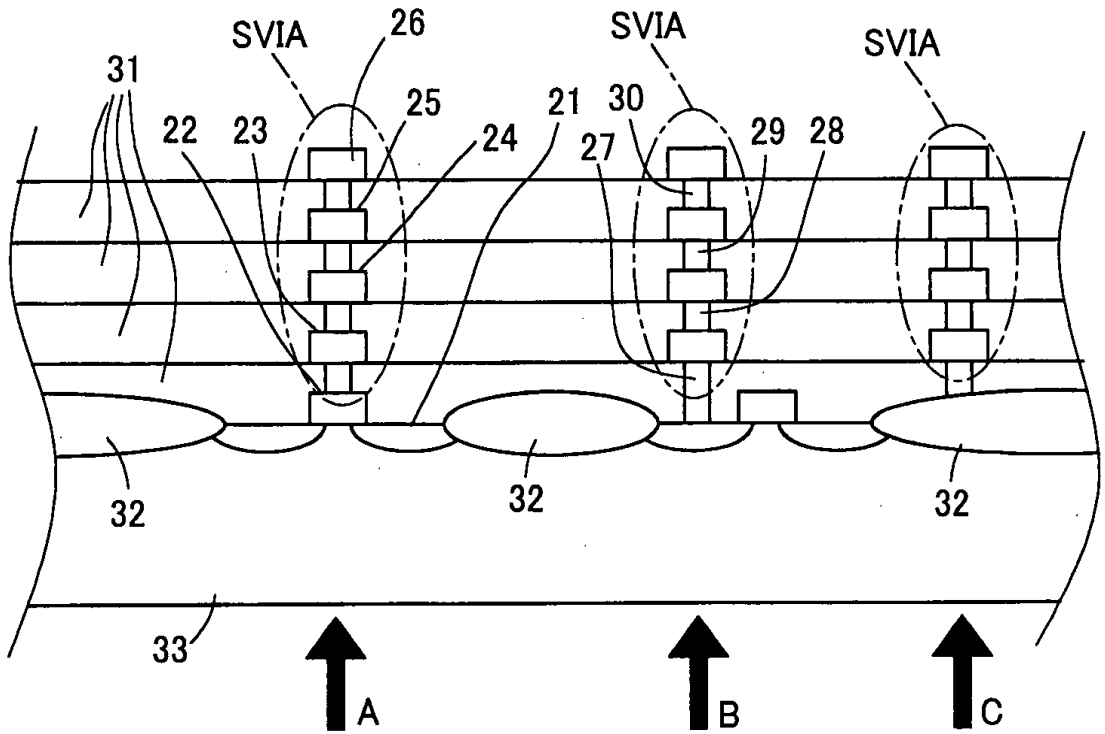


FIG. 10 PRIOR ART

PLAN VIEW SHOWING A CONNECTION BETWEEN METAL WIRING LAYERS IN CONVENTIONAL TECHNOLOGY

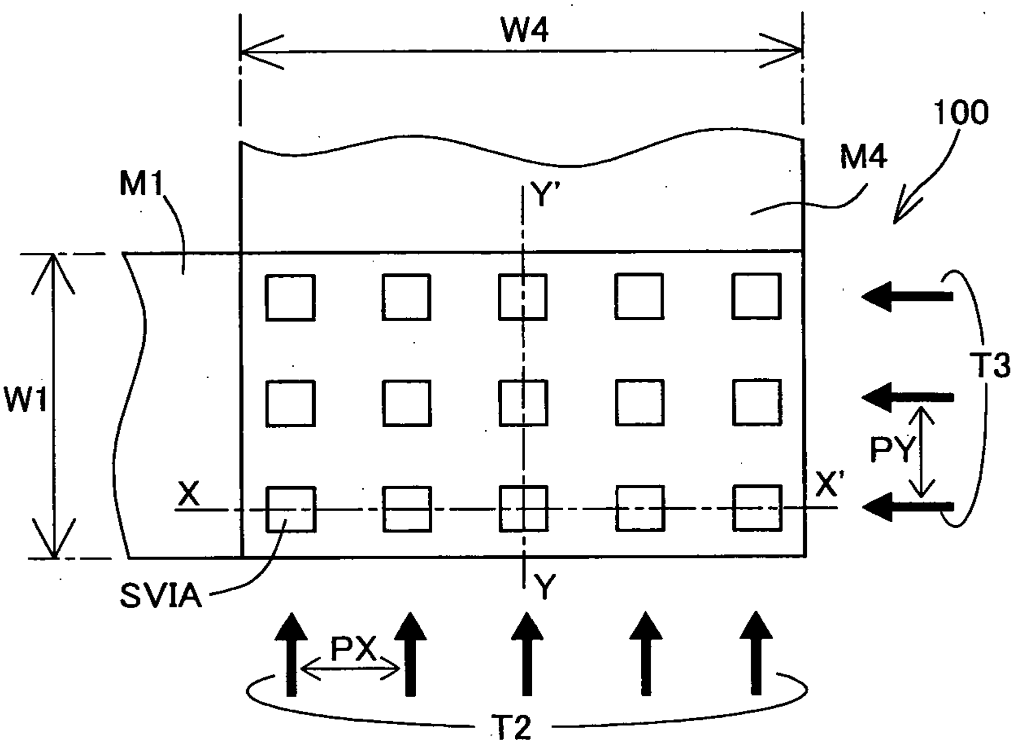


FIG. 11 PRIOR ART

CROSS-SECTIONAL VIEW SHOWING A CONNECTION BETWEEN METAL WIRING LAYERS IN CONVENTIONAL TECHNOLOGY

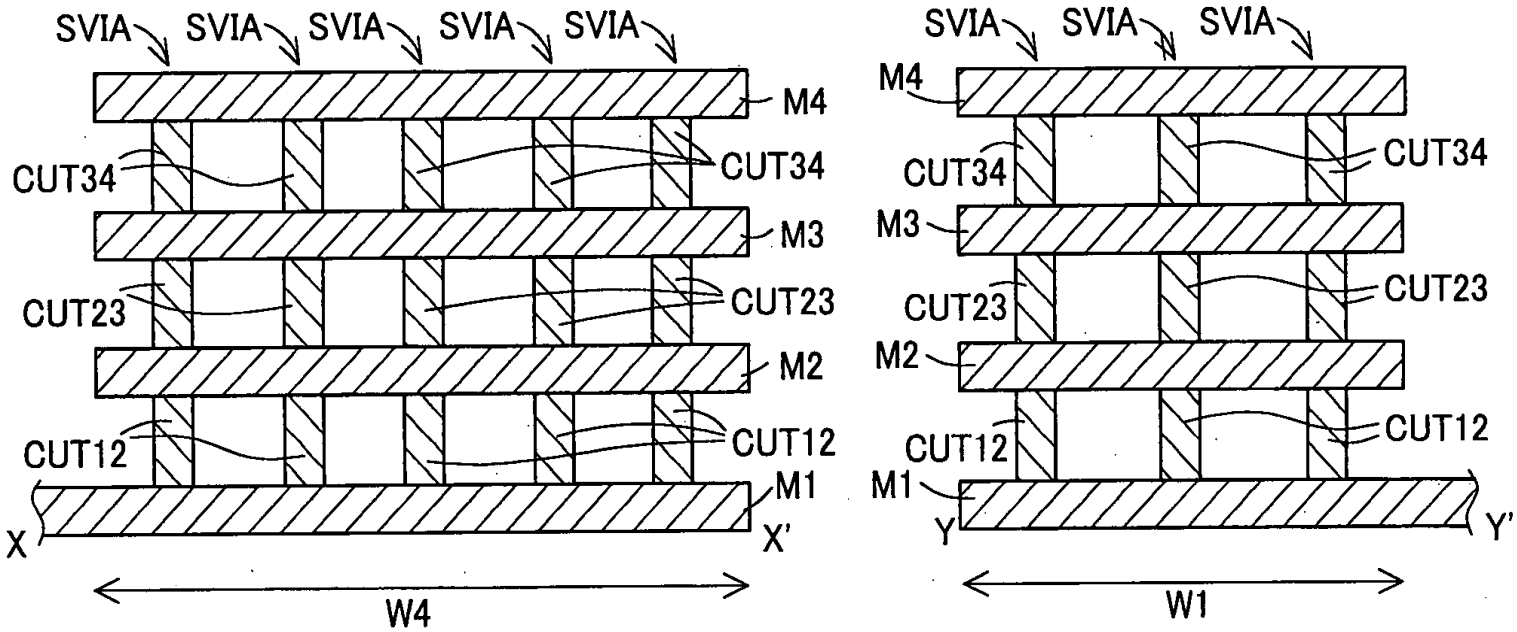


FIG. 12 PRIOR ART

VIEW OF A BASIC MINIMUM PATTERN OF A VIA

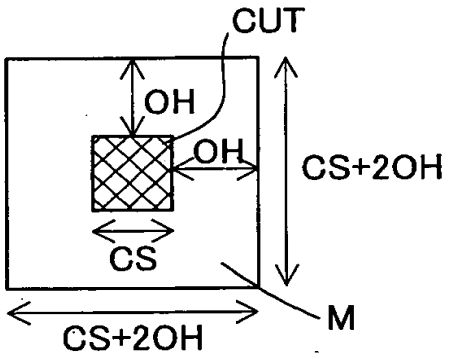
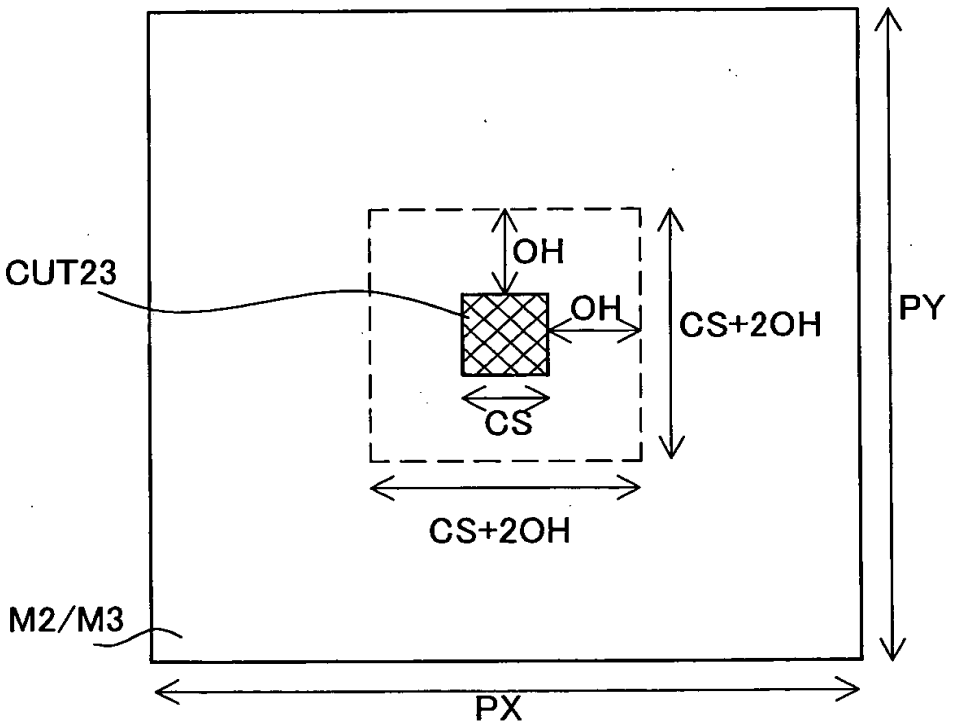


FIG. 13 PRIOR ART

PATTERN VIEW SHOWING AN INTERMEDIATE LAYER VIA IN CONVENTIONAL TECHNOLOGY



(VIA23 = M2 + CUT23 + M3)